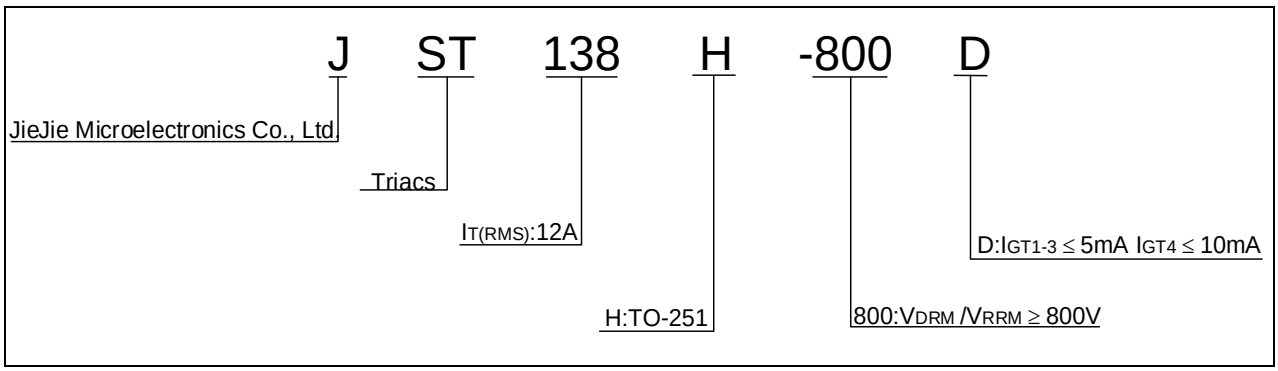
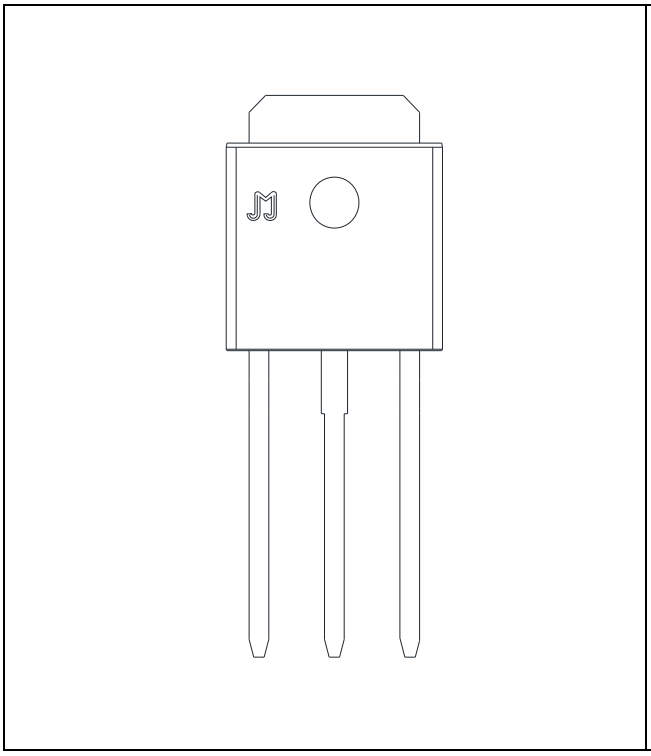
tg	-40-150		

(T_j=25 unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	V_D=12V R_L=33Ω	- -	MAX.	5	mA
				10	
V_{GT}		ALL	MAX.	1	V
V_{GD}	V_D=V_{DRM} T_j=125 R_L=3.3kΩ	ALL	MIN.	0.2	V
I_L	I_G=1.2I_{GT}	- -	MAX.	15	mA
				20	
I_H	I_T=500mA		MAX.	10	mA
dV/dt	V_D=540V Gate Open T_j=125		MIN.	40	V/μs
(dV/dt)c	(dI/dt)c=5A/ms, T_j=110		MIN.	2	V/μs
t_{on}	I_G=20mA I_A=200mA I_R=20mA T_j=25		TYP.	3	


J
ST
138
H
-800
D
JieJie Microelectronics Co., Ltd
Triacs
IT(RMS):12A
H:TO-251
800:VDRM /VRRM ≥ 800V
D:IGT1-3 ≤ 5mA IGT4 ≤ 10mA



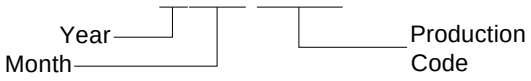
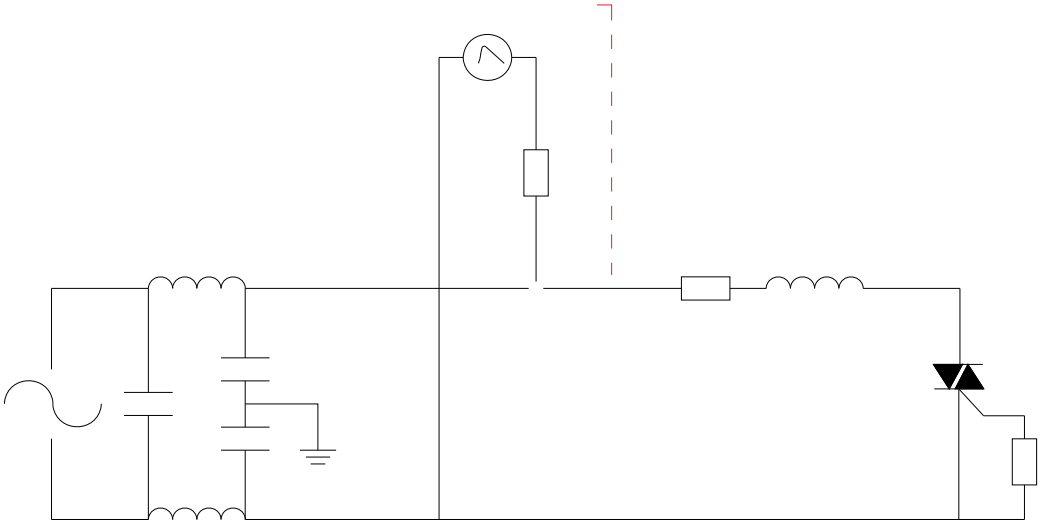
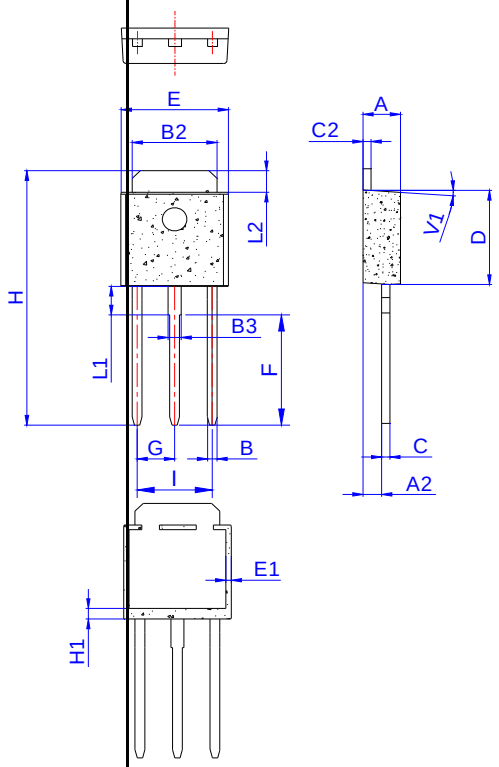

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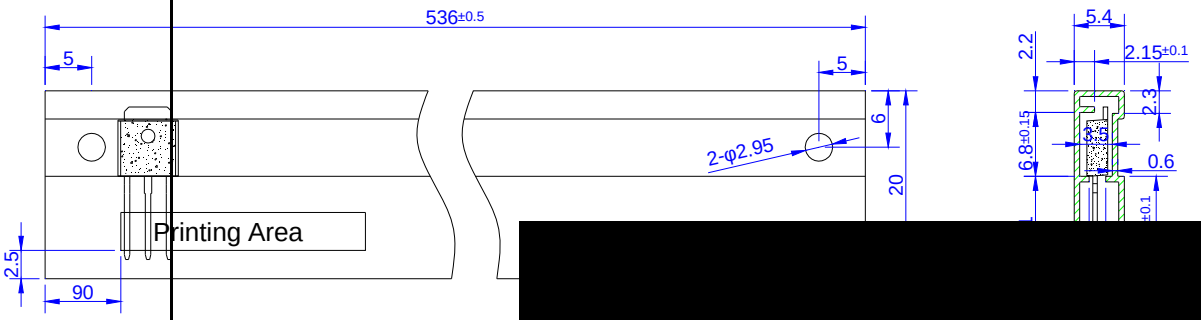
FIG.1:

FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards





Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.20		2.40	0.086		0.095
A2	1.00		1.30	0.039		0.051
B	0.50		0.70	0.020		0.028
B2	5.10		5.40	0.200		0.213
B3	0.70		1.00	0.028		0.039
C	0.45		0.62	0.018		0.024
C2	0.48		0.62	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.70	0.252		0.264
E1	0.60		1.00	0.024		0.039
F	6.90		7.30	0.272		0.287
G	2.20		2.40	0.087		0.094
H	16.00		17.00	0.630		0.669
H1	1.45		1.85	0.057		0.073
I	4.40		4.80	0.173		0.189
L1	1.80		2.20	0.071		0.087
L2	1.25		1.55	0.049		0.061
V1		4°			4°	



PACKAGE

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