JST41T-800BW 40

Peak gate power	P_{GM}	40	W
Peak pulse voltage (T_j=25 ; non-repetitive,off-state;FIG.7)	V_{pp}	1.5	kV

(T_j=25 unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	V_D =12V R_L =33Ω	- -	MAX.	50	mA
V_{GT}		- -	MAX.	1.3	V
V_{GD}	V_D =V_{DRM} T_j=125 R_L =3.3kΩ	- -	MIN.	0.2	V
I_L	I_G=1.2I_{GT}	-	MAX.	80	mA
				200	
I_H	I_T =500mA		MAX.	100	mA
dV/dt	V_D=540V Gate Open T_j=125		MIN.	2000	V/μs

J ST 41 T -800 BW

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Triacs

$I_{T(RMS)}$:40A

T:TG-C(Ins)

800:V_{DRM} /V_{RRM} 800V

BW:I_{GT1-3} 50mA

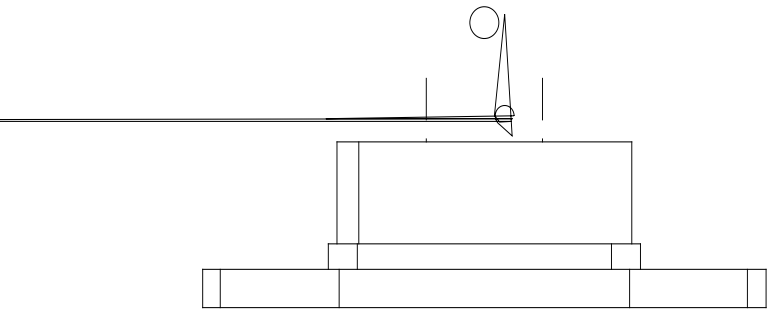
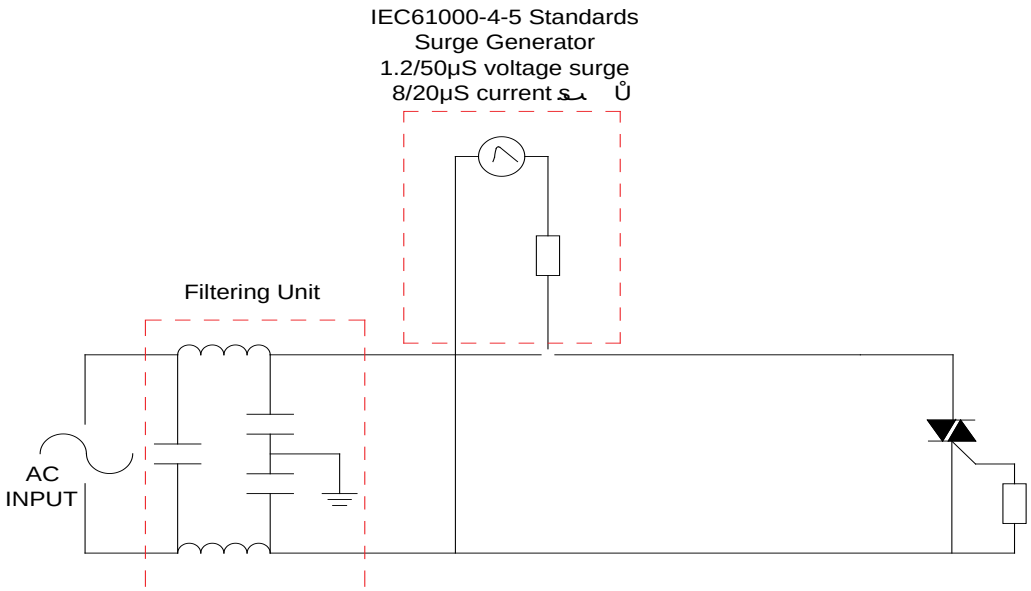


FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards



Order code	Voltage V_{DRM}/V_{RRM}(V)	IGT(mA)	Package	Base qty. (pcs)	Delivery mode
		- -			
JST41T-800BW	800	50	TG-C(Ins)	10	Tube

Document Revision History

Date	Revision	Changes
Apr.11, 2023	A.1.0	

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